PATENT APPLICATION

HEWLETT-PACKARD COMPANY
Legal Department, 20BN
P.O. Box 10301
Palo Alto, California 94303-0890

ATTORNEY DOCKET NO. 10950486-8

IN THE
U.S. PATENT AND TRADEMARK OFFICE

Anticipated Classification of this application:
Class _____ Subclass _____

Prior application:
Examiner: J. Guay
Art Unit: 2503

"Express Mail" label no.: EE362171842US
Date of Deposit: 10/9/98

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

By _____
Typed Name: Dianna Baker

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

REQUEST FOR A CONTINUING APPLICATION UNDER 37 CFR 1.53(b)

Sir:

This is a request for filing a continuing application under 37 CFR 1.53(b) a
( ) continuation application of:
(X) divisional application of:

Pending Prior Application

Application Serial No 08/802,183 filed 2/18/97.

Title Minority Carrier Semiconductor Devices With Improved Reliability

Name of applicant(s) Stephen A. Stockman, et al.

Copy of Application

(X) Enclosed is a copy of the prior application, including the drawings.
( ) Enclosed is a new specification, including new drawings.

Oath or Declaration

(X) Copy from a prior application (37 CFR 1.63(d)
( ) Newly executed (original or copy)

Foreign Priority - 35 USC 119

( ) Foreign priority under 35 U.S.C. 119 has been claimed in prior application Serial No. _____ filed on _____ in _____

( ) The certified copy has been filed in prior application Serial No. _____ filed _____.

( ) A separate paper claiming direct priority to a foreign application is enclosed herewith. A certified copy of the foreign application will be provided in due course.

Relate Back - 35 USC 120

(X) Amend the specification after the title by inserting the following heading:
--Cross Reference To Related Application(s)--;
and add the paragraph:
--This is a ( ) continuation (X) divisional
of copending application serial number 08/802,183 filed on 2/18/97.

CONTINUING APPLICATION UNDER 37 CFR 1.53(b) (continued)

ATTORNEY DOCKET NO. 10950486-8

Inventorship Statement

( ) Delete the following named individuals as inventors in this application in accordance with 37 CFR 1.53(b) as a result of a change in the claimed subject matter:

Appointment of Associate Attorney

( ) Recognize as Associate Attorney or Agent James C. Pintner
Registration No. 33,272

(X) authorization is hereby granted by signature below of the Attorney or Agent of record

( ) the Associate Attorney or Agent shall not have the authority to appoint other Attorneys or Agents

Communications

(X) Address all future communications to:

Records Manager
Legal Department, 20BN
HEWLETT-PACKARD COMPANY
P. O. Box 10301
Palo Alto, California 94303-0890

Direct telephone calls to:

Pamela Lau Kee
36,184

Other Amendments

(X) Before calculating the filing fee, amend the prior application as follows:

(X) Cancel the following claims 2-20 of the prior application before calculating the filing fee. (At least one original independent claim must be retained for filing purposes).

(X) Enter the enclosed Preliminary Amendment.

Fee Calculation

(X) The filing fee is calculated below for (X) Utility ( ) Design

CLAIMS AS FILED BY OTHER THAN A SMALL ENTITY				
(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) TOTALS
TOTAL CLAIMS	20 — 20	0	X $ 22	$ 0
INDEPENDENT CLAIMS	3 — 3	0	X $ 82	$ 0
ANY MULTIPLE DEPENDENT CLAIMS	0		$ 270	$ 0
BASIC FEE: Design ($330.00); Utility ($790.00)				$ 790
TOTAL FILING FEE				$ 790
TOTAL CHARGES TO DEPOSIT ACCOUNT				$ 790

Charge $ 790 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16, 1.17, 1.19, 1.20 and 1.21. A duplicate copy of this transmittal letter is enclosed.

Respectfully submitted,
Stephen A. Stockman, et al.

By Pamela Lau Kee
Pamela Lau Kee
Attorney/Agent for Applicant(s)
Reg. No. **36,184**

Date: 9 October 1998

Telephone No.: **408-553-3059**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR(S): Stephen A. Stockman, et al.

SERIAL NO: Unknown **Examiner:** Unknown

FILING DATE: Unknown **Group Art Unit:** Unknown

TITLE: Minority Carrier Semiconductor Devices With Improved Stability

THE ASSISTANT COMMISSIONER OF PATENTS
WASHINGTON, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Please delete claims 2-20. Please add the following claims:

1. (Amended) A minority carrier semiconductor device comprising:

an active region [wherein the] with a predefined minority carrier recombination lifetime [is maximized];

at least one conductive region adjacent [to] the active region, wherein the [adjacent] region is [being] doped with an compensating impurity [from the group of deep level impurities, reactive impurities, and shallow compensating impurities], the [doped] adjacent conductive region maintaining the [maximized] predefined minority carrier recombination lifetime [in the active region] during device operation;

semiconductor contact layers; and

electrical contacts [regions], applied to the semiconductor contact layers [device].

21. The device, as defined in claim 1, wherein the compensating impurity is a shallow-level impurity.

22. The device, as defined in claim 21, wherein:

the active region is a III-V semiconductor material;

the adjacent conductive region is a p-type III-V semiconductor material; and

the shallow-level impurity is selected from a group that includes Group IV-B and Group VI-B elements.

23. The device, as defined in claim 1, wherein the compensating impurity is selected from a group that includes Cr, Fe, Co, Cu, and Au.

24. The device, as defined in claim 1, wherein:

the active region is a light emitting region; and

the adjacent conductive region is an injection layer.

25. The device, as defined in claim 1, wherein:

the active region is a light emitting region of a double heterostructure light emitting device; and

the adjacent region is a confining layer of the double heterostructure light emitting device.

26. The device, as defined in claim 25, wherein the doped region has a concentration of the compensating impurity that exceeds $1x10^{16}$ cm^{-3}.

27. A light emitting semiconductor device comprising:

a substrate;

two confining layers, positioned over the substrate, wherein at least one of the two confining layers is doped with a compensating impurity, wherein the doped confining layer remains conductive and decreases the loss of radiative recombination efficiency that occurs during operation;

an active region operative to generate light, having a radiative recombination efficiency, interposing the two confining layers;

a window layer, positioned over the two confining layers; and

a first and a second contact, the first contact electrically connecting to the substrate, the second contact electrically connecting to the window layer.

28. The device, as defined in claim 27, wherein the compensating impurity is a shallow-level impurity.

29. The device, as defined in claim 28, wherein:

the active region is a III-V semiconductor material; and

one of the two confining layers is a p-type III-V semiconductor material, the p-type confining layer being doped with a compensating shallow-level impurity selected from a group that includes Group IV-B and Group VI-B elements.

30. The device, as defined in claim 27, wherein the compensating impurity is selected from a group that includes Cr, Fe, Co, Cu, and Au.

31. The device, as defined in claim 27, wherein one of the two confining layers is p-type, the p-type confining layer having a doping concentration of the compensating impurity that exceeds $1x10^{16}$ cm^{-3}.

32. The device, as defined in claim 31, wherein the doping concentration of the compensating impurity is less than the concentration of the p-type dopant.

33. A method for manufacturing a light emitting semiconductor device comprising the steps of:

fabricating a first confining layer on a substrate;

growing an active region on the substrate, the active region having a radiative recombination efficiency;

fabricating a second confining layer on the active region;

doping the second confining layer with a compensating impurity, wherein the doped confining layer remains conductive and decreases the loss of radiative recombination efficiency that occurs during operation;

growing a window layer over the second confining layer; and

fabricating electrical contacts to the substrate and the window layer.

34. The method, as defined in claim 33, wherein the compensating impurity is a shallow-level impurity.

35. The method, as defined in claim 34, wherein the device is a III-V semiconductor, the second confining layer is p-type, and the compensating impurity is selected from a group that includes Group IV-B and Group VI-B elements.

36. The method, as defined in claim 33, wherein the compensating impurity is a deep-level impurity selected from a group that includes Cr, Fe, Co, Cu, and Au.

37. The method, as defined in claim 33, wherein the active region is a light emitting region of a light emitting device and the second confining layer is an injection region of the light emitting device.

38. The method, as defined in claim 33, wherein the active region is a light emitting region of a double heterostructure device, and the second confining layer is a confining layer of a double heterostructure device.

39. The method, as defined in claim 38, wherein the second confining layer has a doping concentration of the compensating impurity that exceeds $1x10^{16}$ cm^{-3}.

Conclusion

If the Examiner has any further questions or would like to discuss this application in more detail, he is invited to call the applicants' agent at the telephone number given below. The applicants respectfully suggest that the claims presently in the application are distinct over the prior art and that the application is now in condition for allowance. Accordingly, the applicants solicit favorable action.

Respectfully submitted,

Stephen A. Stockman, et al.

Pamela Lau Kee

Pamela Lau Kee
Patent Reg. No. 36,184

October 9, 1998
Hewlett-Packard Company
Legal Department, M/S 20BN
P.O. Box 10301
Palo Alto, CA 94303-0890
(408) 553-3059

MINORITY CARRIER SEMICONDUCTOR DEVICES WITH IMPROVED STABILITY

Background of the Invention

This invention is in the field of minority carrier semiconductor devices. The invention relates in particular to methods for improving the operating stability of light emitting semiconductor devices by the intentional introduction of impurities and the devices created using these methods.

Degradation of semiconductor minority carrier devices typically involves an increase in the non-radiative recombination efficiency of the device during the device's operation. The causes of this degradation depend on the type of device, its structure, materials, and operating conditions.

A known double heterostructure light emitting diode ("LED") is shown in Fig. 1. LED 10 is comprised of an optically transparent GaP window/current spreading/contact layer 12, high bandgap AlInP upper confining/injection layer 14, a lower bandgap $(Al_xGa_{1-x})_{.5}In_{.5}P$ active layer 16, high bandgap AlInP lower confining/injection layer 18, and conductive substrate 20, which may be formed from GaAs or GaP. P-type contact 21 and n-type contact 23 complete the LED. Light extraction occurs through both the top surface and sides of the LED. The layers are generally doped so that the p-n junction is located near or within the active layer, and ohmic contacts 21 and 23 are made to the p-type and n-type regions of the device. The structure may be grown by any of a variety of methods including metal-organic chemical vapor deposition("MOCVD"), vapor phase epitaxy("VPE"), liquid phase epitaxy("LPE"), molecular beam epitaxy("MBE"), and others.

Fig. 2 is an energy band diagram of the LED shown in Fig. 1. When forward biased, efficient injection of the minority carriers into active layer 16 is achieved by careful placement of the p-n junction. The minority carriers are confined within the active layer of the LED by high bandgap confining layers 14 and 18. The recombination process consists of both

radiative recombination which produces the desired light emission and non-radiative recombination, which does not produce light. Non-radiative recombination may result from crystal imperfections within the LED as well as other causes. Light is extracted from the LED through the LED's various transparent layers and surfaces and is focussed into a usable pattern by various reflectors and lenses(not shown).

The LED illustrated in Fig. 1 is only one example of a minority carrier device. A variety of other minority carrier devices, including bipolar transistors, photodetectors, and solar cells operate on similar physical principles. Semiconductor lasers often have a double heterostructure and similarly experience the competition between radiative and non-radiative recombination. The performance and stability of all these devices depends upon maintaining a long carrier recombination lifetime throughout the operating life of the device.

For the LED of Fig. 1, the output power is directly proportional to the internal quantum efficiency and can be expressed as:

$$\eta_{external} \propto \eta_{internal} \propto [1+(\tau_r/\tau_{nr})]^{-1},$$

where $\eta_{internal}$ is the internal quantum efficiency, $\eta_{external}$ is the external quantum efficiency, τ_r is the radiative recombination lifetime, and τ_{nr} is the non-radiative recombination lifetime. τ_{nr} is inversely related to the number of non-radiative recombination centers in the active region. The relationship $\eta_{external}$ and the concentration of non-radiative recombination centers is illustrated by the graph shown in Fig. 3, which shows the external quantum efficiency $\eta_{external}$ decreasing as the concentration of non-radiative recombination centers increases. A variety of crystal defects can act as non-radiative recombination centers, including substitutional or interstitial impurities such as Cr, Cu, Au, Fe, O and even such shallow dopants as Si, S, Se, native point defects such

as self-interstitials and vacancies, impurity or dopant related complexes and precipitates, surface and interface states, and dislocations and other extended defects. These defects can arise during the growth process due to incorporation of residual impurities or epitaxial defect formation.

A minority carrier device can degrade during operation for several reasons. In an LED, the carrier injection efficiency or light extraction efficiency can change depending on the particular device structure and the operating conditions. The most common cause of decreased device efficiency is an increase in the non-radiative recombination efficiency caused by the formation of defects in the active region during stress. This process results in the gradual degradation of device characteristics over time, as illustrated by the graph shown in Fig. 4. The graph shows that $\eta_{external}$, the external quantum efficiency, decreases as the period of time the device is under stress increases.

A variety of physical processes contribute to the increase in non-radiative recombination centers in the active region during LED operation. Recombination enhanced or photo-enhanced defect reactions within the active region or at nearby edges or interfaces can contribute to the increase. Other processes include the diffusion or propagation of impurities, native point defects, dopants, and dislocations(also known as dark line defects) into the active layer from other regions of the device. These defects and residual or unintentional impurities have always been considered as detrimental to device performance and great efforts have been expended trying to minimize the concentration of these defects and impurities.

Summary of the Disclosure

A first preferred embodiment of the present invention comprises a method for improving the operating stability of minority carrier semiconductor devices by the intentional introduction of impurities into the layers adjacent to the active region, which impurities act as a barrier to the degradation process, particularly undesired defect formation and propagation. The semiconductor devices produced using this method also comprise this first embodiment of the invention. In a particular example of this first preferred embodiment, impurities are introduced by intentionally doping III-V optoelectronic semiconductor devices with oxygen("O") during an epitaxial growth step. Normally, O is considered an efficient deep level trap, and undesirable in an optoelectronic device. However, as will be described in more detail below, using O in the manner described herein improves device reliability without loss of device efficiency.

The present invention will now be described in detail with reference to the drawings listed and described below.

Brief Description of the Illustrations

Fig. 1 is a cross-sectional drawing of a known light emitting semiconductor device;

Fig. 2 is an energy band diagram of the light emitting semiconductor device shown in Fig. 1;

Fig. 3 is a graph of the concentration of non-radiative recombination centers versus the external quantum efficiency of the device shown in Fig. 1;

Fig. 4 is a graph of the stress time versus the external quantum efficiency of the device shown in Fig. 1;

Fig. 5 shows the effect of O in the active layer on $\eta_{external}$;

Fig. 6 shows the effect of O in the p-type confining layer on $\Delta\eta_{external}$;

Fig. 7 is a graph showing the concentration of oxygen in each of the layers of a semiconductor device as taught by the

first preferred embodiment of the present invention; and

Fig. 8 is a graph of the external quantum efficiency $\eta_{external}$ of devices constructed according to the present invention versus stress time.

Detailed Description of the Preferred Embodiments

High efficiency visible LEDs can be made using an $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ material system. Such devices are structurally similar to the LED shown in Fig. 1. The substrate is typically either GaAs or GaP, the confining layers are $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ $(0<X\leq1)$, the active layer is $(Al_yGa_{1-y})_{0.5}In_{0.5}P$ $(0\leq Y\leq X)$ and the window layer is an optically transparent and electrically conductive material such as AlGaAs or GaP. The most commonly used epitaxial growth technique for these materials is MOCVD. In these materials, O incorporation occurs easily in the alloys containing Al and leads to undesirable deep level defects which cause efficient non-radiative recombination, resulting in low initial $\eta_{external}$. Several techniques are used to minimize O incorporation in these alloys, including growth at high substrate temperatures, use of a substrate orientation which reduces O incorporation efficiency, and growth with a high phosphorus overpressure(high V/III ratio).

The amount of O in the epitaxial structure has a major impact not only on the LED efficiency, but also on device reliability.

Experiments with independently varying the O concentration in each of the various layers of the epitaxial structure, using intentionally controlled O incorporation, with the O levels being kept low enough so that the O doped layers remain conductive, showed that device efficiency depends on the O concentration in the active region. However, device reliability depends on the amount of O in the p-type confining layer. These results are shown in Figs. 5 and 6. The graph in Fig. 5 indicates that $\eta_{external}$ decreases with increasing O in the active layer. Fig. 6 shows that as O in the p-type confining layer increases, degradation of the LED

is reduced. The trend of decreasing $\eta_{external}$ with increasing O content in the active layer was expected, as O is known to form a deep trap which contributes to non-radiative recombination in the $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ active region. However, the result of improved device stability with increasing O content in the p-type upper confining layer was not expected. These results permit the simultaneous optimization of the device's efficiency and reliability by correctly adjusting the O profile of the epitaxial structure.

As the precise nature of the LED degradation mechanism is unknown, the precise reason that this O doping improves device stability is also unknown. The O may tie up or slow down the propagation of other impurities, native point defects, substitutional or interstitial dopants, or dislocations which would otherwise be free to propagate into the active region from the confining layers, substrate, metal contacts, mismatched interfaces, edges, or epitaxial defects, causing device degradation.

In III-V semiconductor materials, O can be a deep level impurity, a reactive impurity which may getter or passivate other impurities, or a shallow compensating impurity. The improvement in device reliability described herein is due to one or more of these properties. Similar results could be achieved by choosing other typically undesired impurities with similar properties. Other deep level impurities include the transition metals, such as Cr, Fe, Co, Cu, Au, etc. Other reactive impurities which have gettering or passivating properties include H, C, S, Cl, and F. The choice of shallow compensating impurities depends on the conduction type of semiconductor material. In a p-type region, shallow compensating impurities are shallow donors and in an n-type region, shallow compensating impurities are shallow acceptors. In p-type III-V semiconductors, shallow compensating impurities are the elements in columns IVA and VIA of the periodic table, particularly the donors O, S, Se, Te, C, Si, Ge, and Sn.

A schematic diagram of the first preferred embodiment of the present invention is shown in Fig. 7. Some or all of the available methods to minimize O concentration in the structure are used, with emphasis on keeping active layer 16 as O free as possible. In the case of MOCVD, techniques for reducing O include high growth temperature, high P overpressure, proper substrate orientation[(100) misoriented toward (111)A, for example], source purity, reactor cleanliness, leak integrity, etc.

In the case of $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ LEDs, an O doping source is then used to controllably introduce O into the p-type confining layer 14 to improve reliability. Depending on the dominant degradation mechanism and device configuration, other layers may be doped in other devices. The O doping source could be O_2, H_2O, alkoxide sources such as dimethyl aluminummethoxide and/or diethyl aluminumethoxide, or other O bearing compounds. Improved device stability occurs when the p-type confining layer 14 is doped with O at a concentration of at least $1x10^{16}cm^{-3}$ and up to $5x10^{19}cm^{-3}$. Best results occur when p-type confining layer 14 is doped with a concentration of O of about $1x10^{18}cm^{-3}$. The upper limit of O doping in this material system is determined by the conducting/insulating transition in the confining layer. In other devices and material systems these ranges will of course vary. In some applications it may be desirable to vary the O profile within the p-type confining layer.

The careful optimization of the O profile for the device shown in Fig. 7 results in improved device reliability while maintaining high initial $\eta_{external}$. This is illustrated by the graphs shown in Fig. 8 which illustrate how higher concentrations of O in the p-type confining layer 14 result in higher $\eta_{external}$ after stress is applied for an increasing period of time.

In this preferred embodiment, O is introduced as part of the epitaxial growth process. Other methods, such as implantation or diffusion, can also be used.

Before the research which lead to the present invention, O doping of III-V semiconductors was only used for studying O related deep level defects and for growing semi-insulating materials. As stated previously, O in the active region has always been known to lower efficiency. No previously known literature suggested the use of O doping into a confining layer to improve device performance. The teachings of the present invention could further be used in the fabrication of semiconductor lasers, photodetectors, solar cells, bipolar junction transistors and other minority carrier semiconductor devices.

What Is Claimed Is:

1. A minority carrier semiconductor device comprising:

an active region wherein the minority carrier recombination lifetime is maximized;

at least one region adjacent to the active region, the adjacent region being doped with an impurity from the group of deep level impurities, reactive impurities, and shallow compensating impurities, the doped adjacent region maintaining the maximized minority carrier recombination lifetime in the active region during device operation; and

contact regions applied to the device.

2. The device of claim 1 wherein the deep level impurities comprise transition metals comprising at least Cr, Fe, Co, Cu, and Au.

3. The device of claim 1 wherein the reactive impurities comprise at least H, C, S, Cl, O, and F.

4. The device of claim 1 wherein the impurities comprise shallow compensating impurities.

5. The minority carrier semiconductor device of claim 1 wherein the active region comprises a light emitting region of a light emitting diode and the adjacent region comprises an injection region of a light emitting diode.

6. The minority carrier semiconductor device of claim 5 wherein the active region further comprises a double heterostructure light emitting diode and the adjacent region further comprises a confining layer of a double heterostructure light emitting diode.

7. The minority carrier semiconductor device of claim 6 wherein the impurity is O and the doping concentration is between $1x10^{16}cm^{-3}$ and $5x10^{19}cm^{-3}$.

8. A light emitting semiconductor device comprising:
a substrate;
a first confining layer overlying the substrate;
an active region for generating light wherein the radiative recombination efficiency is maximized overlying the first confining layer;
a second confining layer, the second confining layer overlying the active region;
window layer overlying the second confining layer;and
electrical contacts deposited on the substrate and the window layer,
at least one confining layer doped with an impurity from a group of impurities comprising deep level impurities, reactive impurities, and shallow compensating impurities, the doped confining layer decreasing the loss of quantum efficiency that the device experiences under operating stress.

9. The device of claim 8 wherein the deep level impurities comprise transition metals comprising at least Cr, Fe, Co, Cu, and Au.

10. The device of claim 8 wherein the reactive impurities comprise at least H, C, S, Cl, O, and F.

11. The device of claim 8 wherein the impurities comprise shallow compensating impurities.

12. The light emitting semiconductor device of claim 8 wherein the impurity is oxygen, the second confining layer is p-type, and doping concentration of the oxygen in the p-type confining layer is between $1x10^{16}cm^{-3}$ and $5x10^{19}cm^{-3}$.

13. The light emitting semiconductor device of claim 12 wherein the doping concentration of the oxygen in the p-type confining layer is approximately $1x10^{18}cm^{-3}$.

14. In a minority carrier semiconductor device comprising at least an active region and at least one adjacent region, a method for improving the reliability of the device comprising the step of doping the at least one adjacent region with one impurity from the group of deep level impurities, reactive impurities, and shallow compensating impurities, the doping decreasing the degradation in performance that the device experiences under operating stress.

15. The method of claim 14 wherein the deep level impurities comprise transition metals, the transition metals at least comprising Cr, Fe, Co, Cu, and Au.

16. The method of claim 14 wherein the reactive impurities comprise at least H, C, S, Cl, O, and F.

17. The method of claim 14 wherein the impurities comprise shallow compensating impurities.

18. The method of claim 14 wherein the active region comprises a light emitting region of a light emitting diode and the adjacent region comprises an injection layer of a light emitting diode.

19. The method of claim 18 wherein the active region further comprises a double heterostructure light emitting diode and the adjacent region further comprises a confining layer of a double heterostructure light emitting diode.

20. The method of claim 19 wherein the impurity is O and the doping concentration is between $1x10^{16}cm^{-3}$ and $5x10^{19}cm^{-3}$.

Abstract of the Disclosure

A method for improving the operating stability of compound semiconductor minority carrier devices and the devices created using this method are described. The method describes intentional introduction of impurities into the layers adjacent to the active region, which impurities act as a barrier to the degradation process, particularly undesired defect formation and propagation. A preferred embodiment of the present invention uses O doping of III-V optoelectronic devices during an epitaxial growth process to improve the operating reliability of the devices.

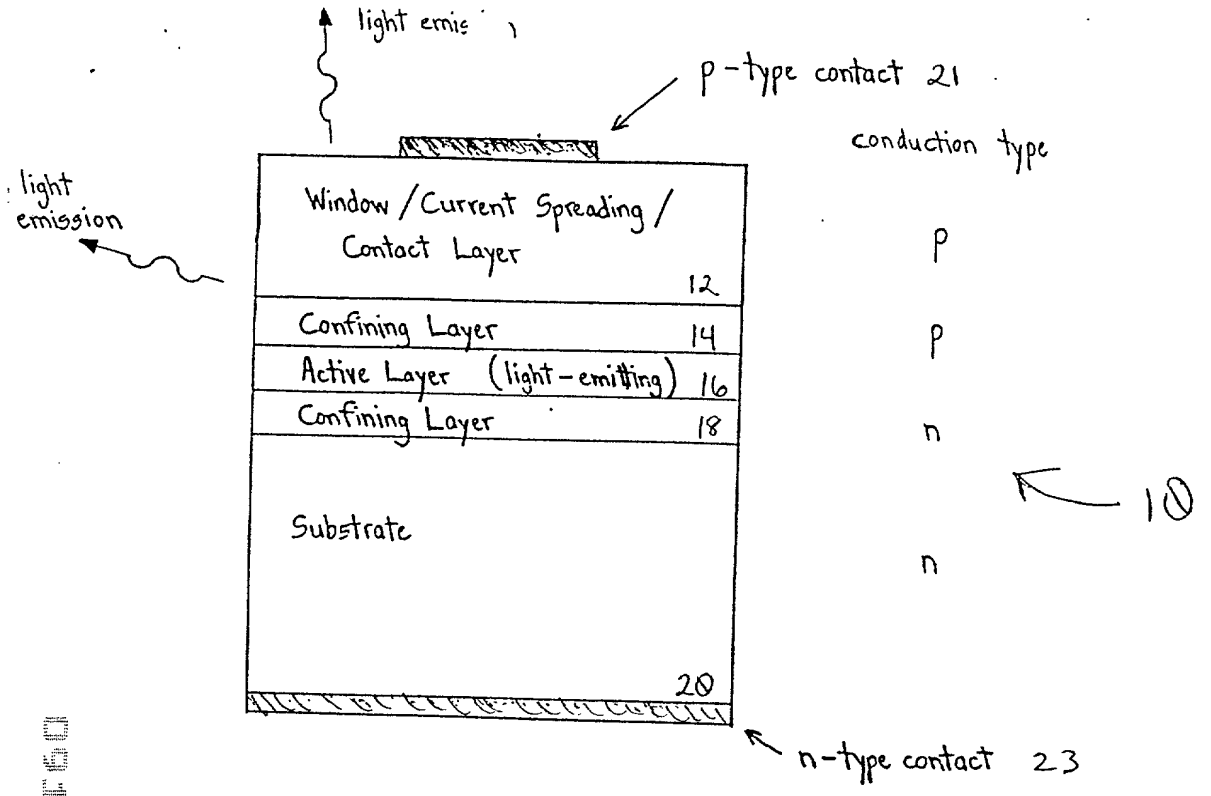


FIGURE 1. Schematic of a double heterostructure light-emitting diode (LED). (Prior Art)

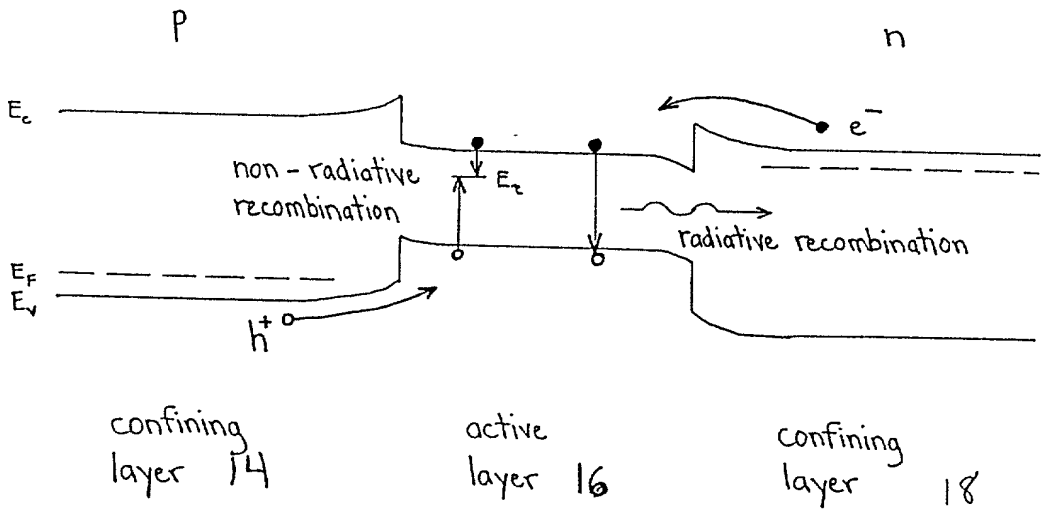


FIGURE 2. Energy band diagram of a double heterostructure LED. (Prior Art)

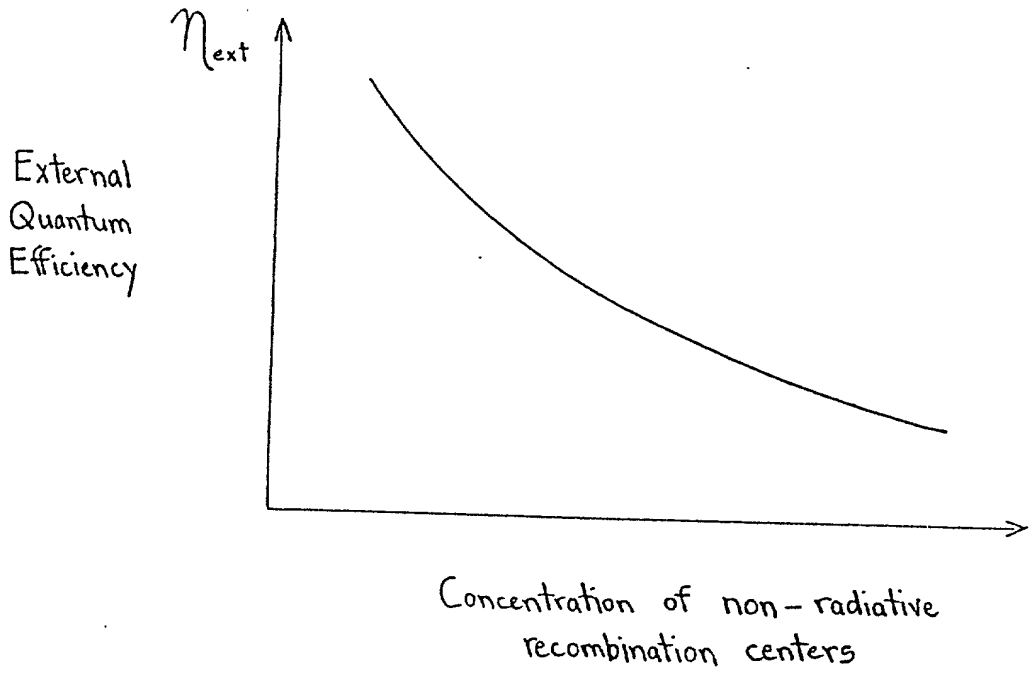


FIGURE 3.

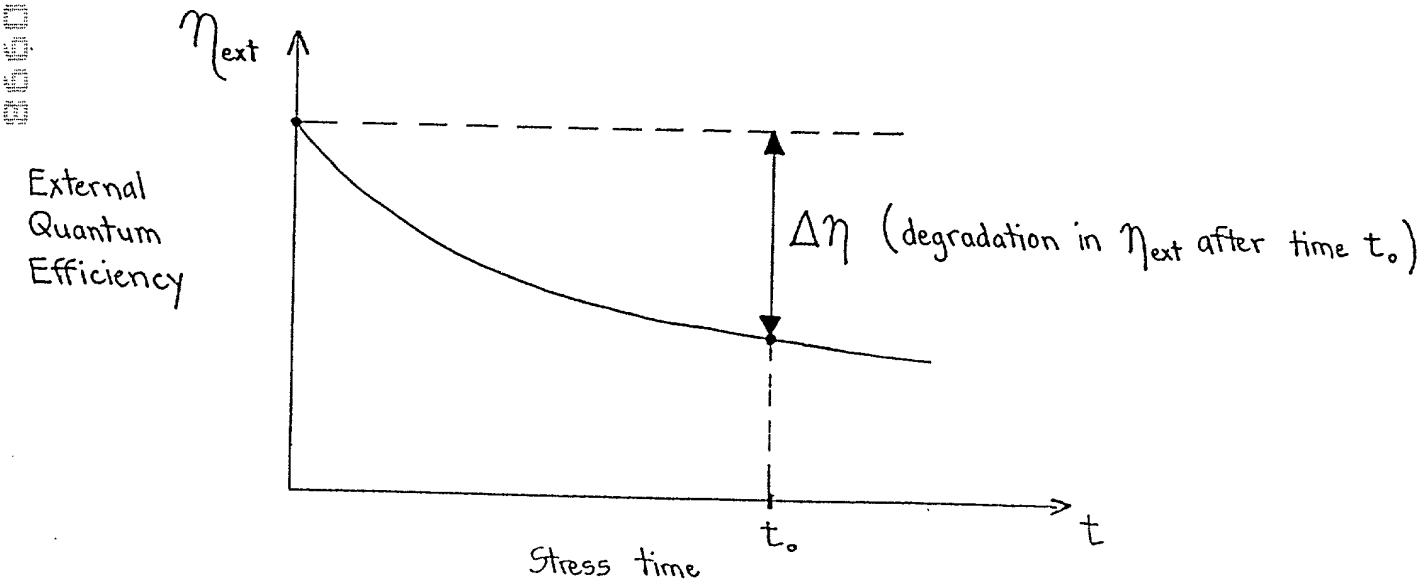
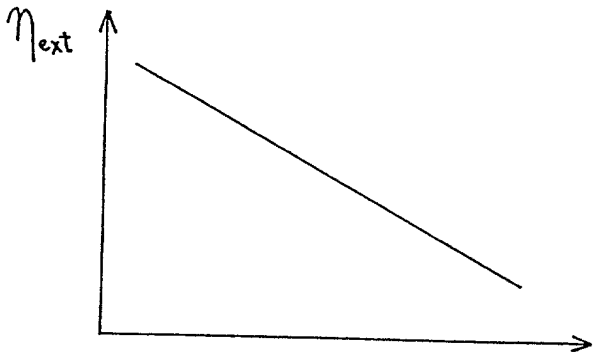


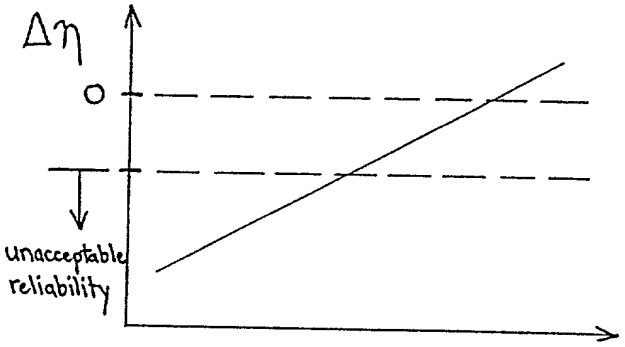
FIGURE 4.

Figure 5



[O] in active layer

Figure 6



[O] in p-type confining layer

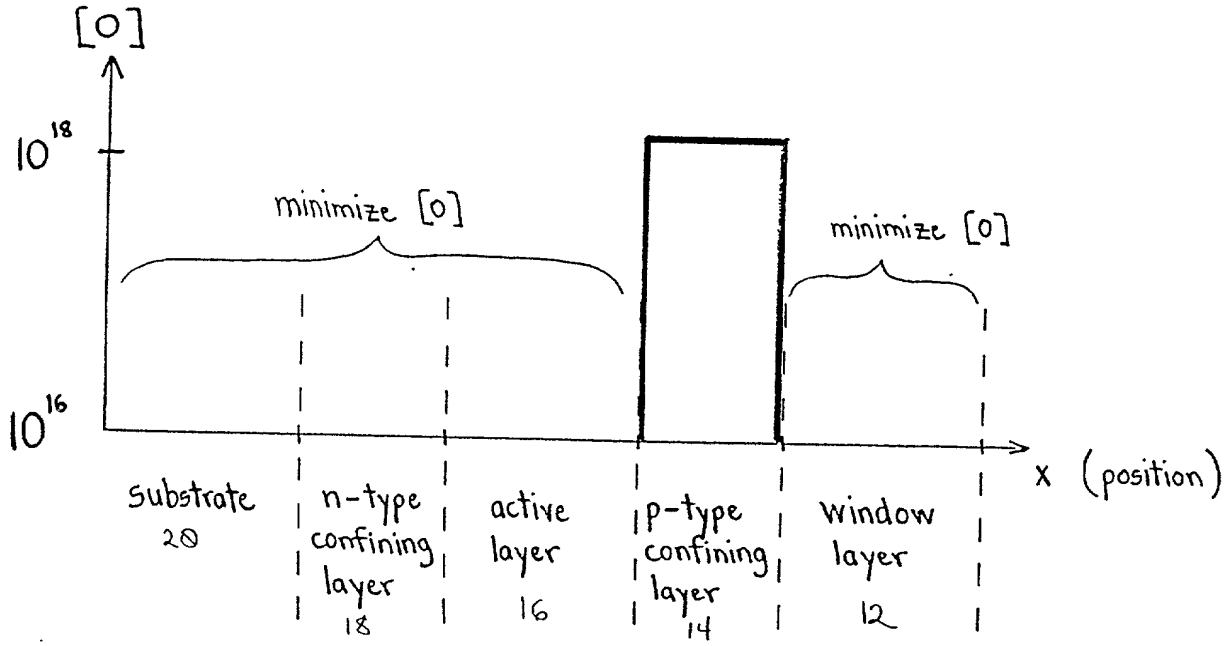


FIGURE 7.

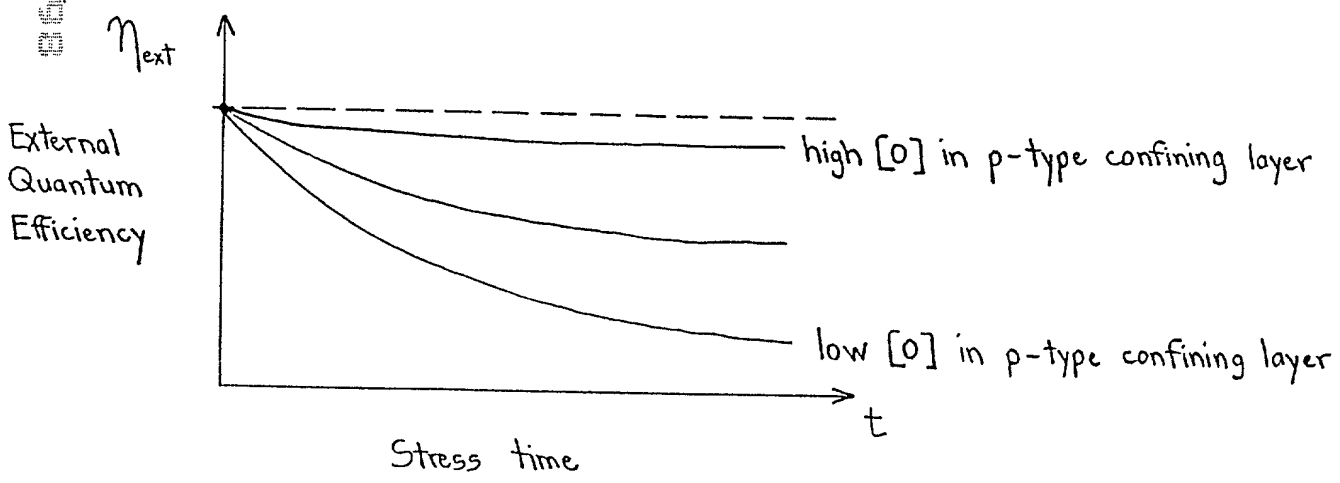


FIGURE 8.

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

ATTORNEY DOCKET NO. 10950486-1

As a below named inventor, I hereby declare that:

My residence/post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Minority Carrier Semiconductor Devices With Improved Stability

the specification of which

(X) is attached hereto. (Leave blank in response to Notice of Missing Parts)

( ) was filed on _____ as Application Serial No._____

( ) was amended by the preliminary amendment filed with the original application papers.

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above and that I have disclosed the best mode for carrying out the invention as of the effective filing date of this application. I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56. If this is a continuation-in-part application, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior (priority) application and the National or PCT international filing date of this continuation-in-part application.

( ) In compliance with this duty there is attached an information disclosure statement 37 CFR 1.97.

Foreign Application(s) and/or Claim of Foreign Priority

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor(s) certificate listed below and have also identified below any foreign application for patent or inventor(s) certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NUMBER	DATE FILED	PRIORITY CLAIMED UNDER 35 U.S.C. 119
			YES: ___ NO: ___
			YES ___ NO: ___
			YES: ___ NO. ___

U. S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (patented/pending/abandoned)

POWER OF ATTORNEY:

As a named inventor, I hereby appoint the attorney(s) and/or agent(s) listed below to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Jonathan B. Penn	Douglas A. Kundrat	Patrick J. Barrett	Pamela Lau Kee
Reg. No. 32,587	Reg. No. 30,275	Reg. No. 26,252	Reg. No. 36,184

Send Correspondence to:
Records Manager
Legal Department, 20BO
HEWLETT-PACKARD COMPANY
P.O. Box 10301
Palo Alto, California 94303-0890

Direct Telephone Calls To:
Jonathan B. Penn
408 553-3053

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willfulfalse statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willfulfalse statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Inventor: Stephen A. Stockman **Citizenship:** US

Residence/Post Office Address: 1402 Pinehurst Square
San Jose, CA 95117

Stephen A. Stockman
Inventor's Signature

June 5, 1995
Date

DECLARATION AND POWER ATTORNEY FOR PATENT APPLICATION (continued)

ATTORNEY DOCKET NO. 10950486-1

Full Name of # 2 joint inventor: Daniel A. Steigerwald Citizenship: US

Residence/Post Office Address: 10414 B Lockwood Dr.
Cupertino, CA 95014

D Steigerwald
Inventor's Signature

5 June 1995
Date

Full Name of # 3 joint inventor: Changhua Chen Citizenship: PRC

Residence/Post Office Address: 4685 Albany Circle, #102
San Jose, CA 95129

Changhua Chen
Inventor's Signature

June 5, 1995
Date

Full Name of # 4 joint inventor: _____ Citizenship: _____

Residence/Post Office Address: _____

_____
Inventor's Signature

_____
Date

Full Name of # 5 joint inventor: _____ Citizenship: _____

Residence/Post Office Address: _____

_____
Inventor's Signature

_____
Date

Full Name of # 6 joint inventor: _____ Citizenship: _____

Residence/Post Office Address: _____

_____
Inventor's Signature

_____
Date

Full Name of # 7 joint inventor: _____ Citizenship: _____

Residence/Post Office Address: _____

_____
Inventor's Signature

_____
Date

Full Name of # 8 joint inventor: _____ Citizenship: _____

Residence/Post Office Address: _____

_____
Inventor's Signature

_____
Date

(Use Next Page For Additional Inventor(s) Signature(s))

Rev 09/93 (Form 3.02)